

3/4/05

**To: Bill Vesperman**

**From: Jeff Harrison, 22511**

**10/616,586**

**Attached are edited 10/616,586, based on subject searching and on forward-citation searching using the related WO/PCT search report in Derwent Patents Citation Index.**

**Please browse the few attached abstracts. I doubt that I found anything close.**

146856

**SEARCH REQUEST FORM Scientific and Technical Information Center - EIC2800**  
 Rev. 3/19/2004 This is an experimental format - Please give suggestions or comments to Jeff Harrison, JEF-4B68, 373-2811.

Date <u>2/24/05</u>	Serial # <u>10/616586</u>	Priority Application Date <u>7-17-2002</u>
Your Name <u>William Veseyman</u>	Examiner # <u>78872</u>	<i>Jefferson</i>
AU <u>2813</u>	Phone <u>571.701</u>	Room <u>TD-30</u>
In what format would you like your results? Paper is the default.		PAPER      DISK      EMAIL

If submitting more than one search, please prioritize in order of need.

The EIC searcher normally will contact you before beginning a prior art search. If you would like to sit with a searcher for an interactive search, please notify one of the searchers.

Where have you searched so far on this case?

Circle:  USPTO  DWPI  EPO Abs  IPO Abs  IBM TDB

Other: \_\_\_\_\_

What relevant art have you found so far? Please attach pertinent citations or Information Disclosure Statements.

20040082147

What types of references would you like? Please checkmark:

Primary Refs  Nonpatent Literature \_\_\_\_\_ Other \_\_\_\_\_  
 Secondary Refs  Foreign Patents \_\_\_\_\_  
 Teaching Refs \_\_\_\_\_

What is the topic, such as the novelty, motivation, utility, or other specific facets defining the desired focus of this search? Please include the concepts, synonyms, keywords, acronyms, registry numbers, definitions, structures, strategies, and anything else that helps to describe the topic. Please attach a copy of the abstract and pertinent claims.

method claim #1 fabricating a composite substrate

forming a recess in the front face of a support or source substrate  
Zone of weakness

transfer layer

bonding material

detaching the transfer layer (mechanically detaching)

- abstract

- specification

SMART

- drawing

support layer

Staff Use Only

Searcher: W. HARRISON

Type of Search

Vendors

Searcher Phone: 22511

Structure (#)

STN

X

Searcher Location: STIC-EIC2800, JEF-4B68

Bibliographic

Dialog

Date Searcher Picked Up: 3-4-05

Litigation

Questel/Orbit

Date Completed: 3-4-05

Fulltext

Lexis-Nexis

Searcher Prep/Rev Time: 31

Patent Family

WWW/Internet

Online Time: 37

Other

Other

DPCT

FILE 'WPIX, JAPIO, HCAPLUS' ENTERED AT 15:35:44 ON 04 MAR 2005

L1           2 S US20040082147/PN  
L2           SEL PLU=ON L1 1- IC RN :         6 TERMS  
L3    147854 S L2  
L4    2 S L1 AND L3  
L5    SEL PLU=ON L4 1- IC MC ECLA IC NCL :         11 TERMS  
L6    154226 S L5  
L7    104 S L6 AND (RECESS##### OR NOTCH##### OR CUTOUT  
          OR CUT OUT) (7A) (TRANSFER##### OR BREAK##### OR SEPARAT#####  
          OR DIVID##### OR DIVISION)  
L8    154226 S L5  
L9    219 S L8 AND (RECESS##### OR NOTCH##### OR CUTOUT  
          OR CUT OUT) (7A) (ADHE##### OR GLU##### OR FIX##### OR  
          POLYMER##### OR BOND##### OR EPOX##### OR RESIN#####)  
L10   12 S L7 AND L9  
L11   50451 S LAYER(3A) TRANSFER#####  
L12   4 S L7 AND L11  
L13   2 S L9 AND L11  
L14   4 S (L12 OR L13) NOT L10  
L15   74619 S (WEAK##### OR FRACTUR##### OR BREAK#####  
          OR BROKEN#####) (5A) (LINE OR AREA OR ZONE OR REGION OR BOUNDARY)  
L16   10565 S DETACH##### (8A) (ALONG OR LINE OR AREA  
          OR ZONE OR REGION OR BOUNDARY)  
L17   73 S (L7 OR L9 OR L11) AND L15  
L18   24 S (L7 OR L9 OR L11) AND L16  
L19   92 S (L17 OR L18)  
L20   68184 S (NOTCH##### OR CUTOUT OR CUT OUT OR  
          RECESS##### OR GROOV#####) (4A) (SUBSTRATE OR SUPPORT#####)  
L21   2 S L19 AND L20

FILE 'DPCI' ENTERED AT 15:50:46 ON 04 MAR 2005

L22   0 S FR2842647/PN  
L23   4 S (FR2811807 OR US2002081822 OR US6406636 OR  
          EP1061566) /PN  
L24   SEL PLU=ON L23 1- PN :         23 TERMS  
L25   12 S L24/PN.D  
L26   21 S L24/PN.G  
L27   33 S L25 OR L26  
L28   SEL PLU=ON L27 1- PN :         166 TERMS  
L29   395 S L28/PN.G  
L30   298 S L28/PN.D  
L31   657 S L29 OR L30  
L32   18 S L31 AND (NOTCH##### OR RECESS##### OR  
          CUTOUT OR CUT OR CUTT#####)  
L33   SEL PLU=ON L32 1- PRN :         28 TERMS

FILE 'WPIX, JAPIO, HCAPLUS' ENTERED AT 15:58:35 ON 04 MAR 2005

L34   43 S L33  
L35   102 S L28  
L36   145 S L34 OR L35  
L37   29 S L36 AND (NOTCH##### OR RECESS##### OR  
          CUTOUT OR CUT OR CUTT#####) (8A) (LAYER OR FILM OR SUBSTRATE OR  
          PLATE OR SLAB OR SUPPORT#####)  
L38   20 S L36 AND (WEAK##### OR FRACTUR##### OR  
          DETACH##### OR BREAK##### OR BROKEN)  
L39   1 S L37 AND L38  
L40   2 S (L37 OR L38) AND FILLER  
L41   1 S (L37 OR L38) AND FILLING  
L42   10 S (L37 OR L38) AND ADHESIVE  
L43   0 S (L37 OR L38) AND GLUE  
L44   1 S (L37 OR L38) AND EPOX#####  
L45   1 S (L37 OR L38) AND RESIN#####  
L46   12 S (L40 OR L41 OR L42 OR L43 OR L44 OR L45)  
          NOT L39

L46 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2005 ACS on STN

AN 2000:589987 HCAPLUS Full-text

DN 133:186471

ED Entered STN: 24 Aug 2000

TI Improved method for depositing semiconductor thin films on porous structures in semiconductor device fabrication

IN Tayanaka, Hiroshi

PA Sony Corp., Japan

SO U.S., 48 pp., Cont.-in-part of U.S. 5,811,348.

CODEN: USXXAM

DT Patent

LA English

IC ICM H01L021-20

NCL 438762000

CC 76-3 (Electric Phenomena)

Section cross-reference(s): 52, 73

FAN.CNT 4

	PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI	US 6107213	A	20000822	US 1997-818239	19970314
	US 5811348	A	19980922	US 1996-595382	19960201 <--
	US 6194239	B1	20010227	US 1999-454552	19991207
	US 6194245	B1	20010227	US 1999-455844	19991207
	US 6326280	B1	20011204	US 2000-616395	20000714 <--
	US 6426274	B1	20020730	US 2000-616613	20000714
PRAI	US 1996-595382	A2	19960201		
	JP 1996-61552	A	19960318		
	JP 1996-234480	A	19960904		
	JP 1995-37655	A	19950202		
	US 1997-818239	A3	19970314		

AB The present invention provides new and improved methods for making crystalline semiconductor thin films which may be bonded to different kinds of substrates. The thin films may be flexible. In accordance with preferred methods, a multilayer porous structure including two or more porous layers having different porosities is formed in a semiconductor substrate. A semiconductor thin film is grown on the porous structure. Electrodes and/or a desired support substrate may be attached to the grown film. The grown film is separated from the semiconductor substrate along a line of **weakness** defined in the porous structure. The separated thin film attached to the support substrate may be further processed to provide improved film products, solar panels and light emitting diode devices. These thin film semiconductors are excellent in crystallinity and may be inexpensively produced, thereby enabling production of solar cells and light emitting diodes at lower cost.

L14 ANSWER 2 OF 4 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 2004-123159 [12] WPIX Full-text

DNN N2004-098483 DNC C2004-049708

TI **Transferring layer** of material from source onto support substrate to form composite substrate for, e.g. optics, involves forming recess(es) to receive excess additional material in the substrate(s) before deposition of additional material.

DC L03 U11

IN ASPAR, B; BRESSOT, S; RAYSSAC, O

PA (COMS) COMMISSARIAT ENERGIE ATOMIQUE; (SOIT-N) SOITEC SILICON ON INSULATOR TECHNOLOGIES; (ASPA-I) ASPAR B; (BRES-I) BRESSOT S; (RAYS-I) RAYSSAC O

CYC 105

PI WO 2004008526 A1 20040122 (200412)\* EN 24 H01L021-762 <--

FR 2842647 A1 20040123 (200416) H01L021-20 <--

US 2004082147 A1 20040429 (200429) H01L021-30 <--

AU 2003250992 A1 20040202 (200450) H01L021-762 <--

ADT WO 2004008526 A1 WO 2003-EP7853 20030716; FR 2842647 A1 FR 2002-9018 20020717; US 2004082147 A1 US 2003-616586 20030709; AU 2003250992 A1 AU 2003-250992 20030716

FDT AU 2003250992 A1 Based on WO 2004008526

PRAI FR 2002-9018 20020717

2004082147, PW,

IC ICM H01L021-20; H01L021-30; H01L021-762

ICS H01L021-18; H01L021-304; H01L021-46

AB WO2004008526 A UPAB: 20040218

NOVELTY - **Transferring a layer** of material from a source substrate onto a support substrate to fabricate a composite substrate involves forming at least one recess for receiving excess additional material in the source and/or support substrates, prior to depositing additional material onto the front face of the substrate(s).

DETAILED DESCRIPTION - **Transferring a layer** of material (41) from a source substrate (4) onto a support substrate (5) to fabricate a composite substrate for applications in the fields of electronics, optics, or optoelectronics involves depositing additional material (6) onto one of the faces, i.e. the front face, of the source substrate and/or onto the front face of the support substrate; applying the source substrate and the support substrate against each other with their respective front faces facing one another; and detaching the **layer** to be **transferred** from the remainder of the source substrate along the zone of weakness (43) by applying a stress of mechanical origin. Prior to the step of depositing the material, at least one recess (56) for receiving excess additional material is formed in at least one of the two substrates. The recess opens onto the front face of the substrate in which it is formed.

USE - The method is used for **transferring a layer** of material, i.e. semiconductor material, from a source substrate onto a support substrate to fabricate a composite substrate for applications in the fields of electronics, optics, or optoelectronics.

ADVANTAGE - The method improves mechanical **layer transfer**, and prevents excess material deposited at the bonding interface between a source substrate and a support substrate from masking the attack edge of the zone of weakness.

DESCRIPTION OF DRAWING(S) - The figure is a diagram illustrating the steps of the **layer transfer** method.

Source substrate 4

Support substrate 5

Additional material 6

Layer of material 41

Zone of weakness 43

Recess 56

Dwg. 6/12

TECH WO 2004008526 A1UPTX: 20040218

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Method: The recess communicates with the rear face of the substrate in which it is formed, and is in the form of an annular groove opening onto the front face of the substrate in which is formed. The recess is formed by wet or dry etching, or by mechanical machining using a saw or a laser beam. The zone of weakness is formed by implanting atomic species, by a porous layer, or by a releasable bonding interface. The **recess** provided in the source substrate is produced prior to the atomic species implantation step.

TECHNOLOGY FOCUS - INORGANIC CHEMISTRY - Preferred Materials: The **layer** to be **transferred** is composed of a semiconductor material. The additional material is an adhesive or an adhesive material.

L10 ANSWER 12 OF 12 HCAPLUS COPYRIGHT 2005 ACS on STN

AN 2002:241312 HCAPLUS Full-text

DN 136:271744

ED Entered STN: 28 Mar 2002

TI Method for efficiently manufacturing semiconductor devices of reduced size

IN Mimata, Tsutomu

PA Kabushiki Kaisha Shinkawa, Japan

SO U.S. Pat. Appl. Publ., 10 pp.

CODEN: USXXCO

DT Patent

LA English

IC ICM H01L021-301

ICS H01L021-46; H01L021-78

NCL 438460000

CC 76-3 (Electric Phenomena)

FAN.CNT 1

PATENT NO.	KIND	DATE	APPLICATION NO.	DATE
PI, US 2002037631	A1	20020328	US 2001-961222	20010921
JP 2002100588	A2	20020405	JP 2000-289513	20000922
PRAI JP 2000-289513	A	20000922		

CLASS

PATENT NO.	CLASS	PATENT FAMILY CLASSIFICATION CODES
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US 20020037631	ICM	H01L021-301
	ICS	H01L021-46; H01L021-78
	NCL	438460000

AB Method for efficiently manufacturing semiconductor devices of reduced size is claimed. A method for manufacturing semiconductor devices comprising a step in which an **adhesive** layer used to **bond** dies **cut out** of a wafer to another member is formed on the front surface of the wafer that has desired integrated circuits, and a step in which a thin film conversion treatment was performed from the back surface side on the wafer in which **recessed** grooves used for **separation** of dies were formed from the front surface side and on which the **adhesive** layer was formed, until the **recessed** grooves are exposed.

ST fabrication semiconductor device adhesive bonding die

IT Adhesive bonding

Adhesive films

Dies

Integrated circuits

(method for efficiently manufacturing semiconductor devices of reduced size)

L10 ANSWER 2 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 2003-577005 [54] WPIX Full-text

DNN N2003-458670 DNC C2003-155886

TI Formation of semiconductor device involves bonding the donor substrate to receiving substrate via donor mesa, and removing bulk portion while leaving transferred layer of donor substrate bonded to receiving substrate.

DC L03 U11

IN CSUTAK, S; JONES, R E

PA (CSUT-I) CSUTAK S; (JONE-I) JONES R E; (MOTI) MOTOROLA INC

CYC 103

PI US 2003114001 A1 20030619 (200354)\* 9 H01L021-302

WO 2003052817 A2 20030626 (200354) EN H01L023-00

RW: AT BE BG CH CY CZ DE DK EA EE ES FI FR GB GH GM GR IE IT KE LS LU

US 6616854 B2 20030909 (200361) C03C015-00

AU 2002353020 A1 20030630 (200420) H01L023-00

EP 1500132 A2 20050126 (200508) EN H01L021-762 <--

R: AL AT BE BG CH CY CZ DE DK EE ES FI FR GB GR IE IT LI LT LU LV MC

MK NL PT RO SE SI SK TR

KR 2004079916 A 20040916 (200508) H01L021-20 <--

ADT US 2003114001 A1 US 2001-22711 20011217; WO 2003052817 A2 WO 2002-US38564

20021205; US 6616854 B2 US 2001-22711 20011217; AU 2002353020 A1 AU

2002-353020 20021205; EP 1500132 A2 EP 2002-789986 20021205, WO

2002-US38564 20021205; KR 2004079916 A KR 2004-710056 20040617

FDT AU 2002353020 A1 Based on WO 2003052817; EP 1500132 A2 Based on WO

2003052817

PRAI US 2001-22711 20011217

IC ICM C03C015-00; H01L021-20; H01L021-302; H01L021-762;

H01L023-00

ICS H01L021-461

AB US2003114001 A UPAB: 20030821

NOVELTY - A semiconductor device is formed by implanting a species into a donor substrate to form implant region, patterning the donor substrate to form bulk portion and donor mesa comprising implant region, bonding the donor substrate to receiving substrate via a donor mesa, and removing the bulk portion while leaving a transferred layer of the donor substrate bonded to receiving substrate.

USE - For forming a semiconductor device.

ADVANTAGE - The method achieves a higher degree of planarity on the final structure. It effectively raises the area of the receiving substrate at area where bonding of another semiconductor material is to occur, thus assuring a sufficient bonding at such area.

DESCRIPTION OF DRAWING(S) - The drawing shows a partial, cross-sectional view of a semiconductor device manufactured by the inventive method.

Receiving substrate 42

Donor substrate 50

Implant region 52

Dwg. 9/11

TECH US 2003114001 A1UPTX: 20030821

TECHNOLOGY FOCUS - ELECTRONICS - Preferred Components: The receiving substrate (42) comprises semiconductor material and first dielectric material. The first dielectric layer has a recess and the transferred layer is bonded within the recess.

A photodetector is formed in the transferred layer. The bulk portion is removed by using mechanical or thermal method.

Preferred Method: A trench is formed within the semiconductor material and the transferred material is bonded within the trench. The implanting step is performed before patterning the donor substrate. The patterning donor substrate (50) includes removing portions of the implant region (52) beyond the mesa.

Preferred Materials: The donor substrate and the receiving substrate comprise germanium, gallium, arsenic, indium, phosphorus, or silicon. The donor substrate comprises single crystalline germanium and the receiving substrate comprises a single crystalline silicon.

FS CPI EPI

FA AB; GI

MC CPI: L04-C12C; L04-C17

EPI: U11-C01J8A; U11-C08A4

L10 ANSWER 3 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 2003-506509 [48] WPIX [Full-text](#)

DNN N2003-402190 DNC C2003-135575

TI Bonded assembly of two wafers is formed using wafer recessed to make penetrations, and results in highly temperature-stable, detachable connection.

DC L03 U11

IN PAIRITSCH, H; RUEB, M

PA (INFN) INFINEON TECHNOLOGIES AG

CYC 1

PI DE 10156465 C1 20030710 (200348)\* 13 H01L021-58

ADT DE 10156465 C1 DE 2001-10156465 20011116

PRAI DE 2001-10156465 20011116

IC ICM H01L021-58

AB DE 10156465 C UPAB: 20030729

NOVELTY - The first and second surfaces (3, 4) of a first wafer (1) are recessed (2, 5) forming penetrations between them, over the entire first surface of the first wafer. A temperature-stable, detachable connection (21) is formed between them, with spacing layers (13-15) of dielectric, uniting the first surface of the first wafer with a first surface of the second wafer, by wafer-bonding connection.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is included for a corresponding method of forming a detachable, highly-temperature stable bond between two wafers.

USE - To bond two wafers together, detachably.

ADVANTAGE - In a simple manner, a highly temperature-stable, detachable connection is prepared between two wafers. Once connected, they can continue to processing using conventional techniques. Conventional machines are used, even when the combined wafer is very thin. The wafers are connected by a silica layer, but are very readily re-separated at low cost, without mechanical damage. The recessed wafer can be re-used following separation, i.e. it need be structured only once.

DESCRIPTION OF DRAWING(S) - The drawing shows a schematic side view of the joined wafers.

First wafer 1

Recesses 2, 5

First and second surfaces 3, 4

Spacing layers 13-15

Detachable connection 21

Dwg. 3/5

FS CPI EPI

FA AB; GI

MC CPI: L04-C17; L04-F

EPI: U11-C01J8A

L10 ANSWER 4 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 2002-414611 [44] WPIX Full-text

DNN N2002-326029

TI Semiconductor device manufacturing method involves forming adhesive layer to front surface of wafer and performing thin film conversion treatment on back surface of wafer, until grooves on wafer are exposed.

DC U11

IN MIMATA, T

PA (SHKW) SHINKAWA KK

CYC 4

PI US 2002037631 A1 20020328 (200244)\* 10 H01L021-301  
 JP 2002100588 A 20020405 (200244) 6 H01L021-301  
 KR 2002023105 A 20020328 (200265) H01L021-78  
 TW 493236 A 20020701 (200329) H01L021-60  
 KR 433781 B 20040604 (200465) H01L021-78

ADT US 2002037631 A1 US 2001-961222 20010921; JP 2002100588 A JP 2000-289513  
 20000922; KR 2002023105 A KR 2001-46155 20010731; TW 493236 A TW  
 2001-117741 20010720; KR 433781 B KR 2001-46155 20010731

FDT KR 433781 B Previous Publ. KR 2002023105

PRAI JP 2000-289513 20000922

IC ICM H01L021-301; H01L021-60; H01L021-78

ICS H01L021-46; H01L025-065

AB US2002037631 A UPAB: 20020711

NOVELTY - An adhesive layer is formed on front surface of a wafer (6), to bond a die cut out from wafer. A thin film conversion treatment is performed on back surface of wafer, where recessed grooves (9) for separation of dies are formed. The thin film formation is performed until the grooves are exposed.

USE - For manufacturing semiconductor devices.

ADVANTAGE - The adhesive layer covers the entire front surface except metal bumps, thus bonding to metal bumps is performed without any hindrance. Both positioning precision of adhesive layer and size reduction of semiconductor layer are performed simultaneously by DBG method. Hence, efficiency of manufacturing process is increased.

DESCRIPTION OF DRAWING(S) - The figure shows a sectional view of semiconductor device.

Wafer 6

Grooves 9

Dwg.1c/5

FS EPI

FA AB; GI

MC EPI: U11-E02A3

L10 ANSWER 6 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 1995-264009 [34] WPIX Full-text

DNN N1995-202943 DNC C1995-120225

TI Mfr. of IC chips from a single wafer - by forming metal contacts on the pre-packaged IC devices while they are still joined together on the wafer..

DC A85 L03 U11

IN BADEHI, P

PA (SHEL-N) SHELLCASE LTD

CYC 64

PI	WO 9519645	A1 19950720 (199534)*	EN 36	H01L023-485
	AU 9514564	A 19950801 (199546)		H01L023-485
	EP 740852	A1 19961106 (199649)	EN	H01L023-485
	R: AT BE CH DE DK FR GB GR IE IT LI NL SE			
	JP 09511097	W 19971104 (199803)	28	H01L021-301
	KR 97700939	A 19970212 (199809)		H01L023-485
	SG 50376	A1 19980720 (199838)		H01L023-485
	EP 740852	B1 19990804 (199935)	EN	H01L023-485
	R: AT BE CH DE DK FR GB GR IE IT LI NL SE			
	MX 9602801	A1 19971201 (199936)		H01L023-485
	DE 69511241	E 19990909 (199943)		H01L023-485
	US 6040235	A 20000321 (200021)		H01L021-301
	TW 360957	A 19990611 (200027)		H01L023-02
	IL 108359	A 20010430 (200134)		H01L021-04

PRAI IL 1994-108359 19940117

AB WO 9519645 A UPAB: 19950904

ICs are mfd. by: forming ICs (40) on a wafer, each IC having contact pads (34); bonding a layer of protective material (26,42) to each wafer surface; cutting notches into the wafer through the protective layer (26) to outline individual IC devices; forming metal contacts (12) on the devices while they are still joined together on the wafer, at least part of the contacts extending into the notches; and separating the wafer into individual IC devices.

Pref. the notch-cutting step exposed sectional surfaces of the IC pads or cuts the pads to define contact regions for two adjacent ICs.

Appts. for producing the ICs by the above method is claimed, including stations for forming the ICs on a wafer, bonding the protective layers, cutting the notches, adding the metal contact layers and separating the wafer into individual ICs along the notch lines.

IC device formed as above is claimed.

ADVANTAGE - IC devices are obtd. which are small in size and weight and have good electrical performance.

Dwg. 7/15

FS CPI EPI

FA AB; GI

MC CPI: A05-A01E2; A12-E07C; L04-F03

EPI: U11-C05G2B; U11-C06A2; U11-D01A; U11-D03B1

PLE UPA 19951011

[1.1] 017; P0464-R D01 D22 D42 F47

[1.2] 017; ND01; ND07; N9999 N7170 N7023; Q9999 Q7374-R Q7330; Q9999 Q7476 Q7330; B9999 B4842 B4831 B4740; N9999 N5721-R; B9999 B4397 B4240; K9790-R

L10 ANSWER 8 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 1992-037018 [05] WPIX [Full-text](#)

DNN N1992-028240 DNC C1992-016345

TI Formation of semiconductor substrath with dielectric **separation**  
regin - by **bonding** substrates with etched **recess** and  
groove followed by oxidation of the internal surface of the voids.

DC L03 U11

IN FUJINO, S; KATADA, M; MATSUI, M; TSURUTA, K

PA (NIJI) NIPPON JIDOSHA BUHIN SOGO; (NSOK) NIPPON SOKEN KK

CYC 2

PI JP 03283636 A 19911213 (199205)\* 5 H01L021-76

US 5223450 A 19930629 (199327)B 14 H01L021-302

ADT JP 03283636 A JP 1990-85257 19900330; US 5223450 A US 1991-678082 19910401

PRAI JP 1990-85257 19900330

IC ICM H01L021-302; H01L021-76

ICS H01L021-304; H01L021-306

AB JP 03283636 A UPAB: 19991011

Method of producing a semiconductor substrate having a buried dielectric layer by bonding between bonding plates of first and second semiconductor substances comprising; a) forming a **recess** of predetermined depth on its **bonding** plane of one of the substrates where its dielectric buried layer is to be formed, and a groove on one of the substrates connecting the recess to the peripheral end face of a corresponding substrate, the depth of the groove being deeper than the **recess**, b) **Bonding** the substrates together, c) Removing damaged parts existing at least at corners where groove and recess meet and along the groove and **recess**. d) Oxidising by exposing the **bonded** substrates to an oxidising gas and channelling the gas flow along the groove growing an oxide film over an inner wall of the recess to form a buried dielectric layer.

Also carried is the method in which the groove is formed before the recess. Also claimed is a method in which plurality of grooves, are formed in a grid formation.

Also claimed is the method in which the oxide film and damage removing step are carried out before bonding the substrates.

USE/ADVANTAGE - The method selectively and securely forms a dielectric buried layer in substrates which have been directly bonded. (First major country equivalent to J03283636-A)

ABEQ US 5223450 A UPAB: 19931116

Method of producing a semiconductor substrate having a buried dielectric layer by bonding between bonding plates of first and second semiconductor substances comprising; a) forming a **recess** of predetermined depth on its **bonding** plane of one of the substrates where its dielectric buried layer is to be formed, and a groove on one of the substrates connecting the recess to the peripheral end face of a corresponding substrate, the depth of the groove being deeper than the **recess**, b) **Bonding** the substrates together, c) Removing damaged parts existing at least at corners where groove and recess meet and along the groove and **recess**. d) Oxidising by exposing the **bonded** substrates to an oxidising gas and channelling the gas flow along the groove growing an oxide film over an inner wall of the recess to form a buried dielectric layer.

Also carried is the method in which the groove is formed before the recess. Also claimed is a method in which plurality of grooves, are formed in a grid formation.

Also claimed is the method in which the oxide film and damage removing step are carried out before bonding the substrates.

USE/ADVANTAGE - The method selectively and securely forms a dielectric buried layer in substrates which have been directly bonded. (First major country equivalent to J03283636-A)

Dwg.4/19

FS CPI EPI

FA AB; GI

MC CPI: L04-C12C

EPI: U11-C05B1; U11-C08A3

L10 ANSWER 9 OF 12 JAPIO (C) 2005 JPO on STN

AN 2003-124167 JAPIO Full-text

TI WAFER SUPPORT MEMBER AND DOUBLE-ENDED GRINDING DEVICE USING THE SAME  
IN ISOBE AKIRA; TOMITA YOSHIYUKI; IWASE AKIO; HARA KAZUTAKA; FURUKAWA RYUJI;  
NAGATA HIROSHI; TSUKAHARA SHINICHIRO

PA SUMITOMO HEAVY IND LTD

PI JP 2003124167 A 20030425 Heisei

AI JP 2001-313010 (JP2001313010 Heisei) 20011010

PRAI JP 2001-313010 20011010

SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2003

IC ICM H01L021-304

ICS B24B007-17; H01L021-68

AB PROBLEM TO BE SOLVED: To provide a wafer support member which can be favorably used for a double-ended grinding device adopting a carrier method, manufactured at a low cost and readily handled.

SOLUTION: This wafer support supports a wafer W having a **notch** portion WN by disposing a plurality of **divided** support members 10A-10C in the outer periphery of the wafer W. Of these divided support members 10A-10C, one having a protrusion 10a engaged with the **notch** portion WN of the wafer W is **fixed** to a carrier, and at least one of the other divided support members 10A-10C is made movable.

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L10 ANSWER 10 OF 12 JAPIO (C) 2005 JPO on STN  
AN 2001-274128 JAPIO Full-text  
TI METHOD OF POLISHING AND PROCESSING THIN SHEET, AND METHOD OF MANUFACTURING  
PIEZOELECTRIC VIBRATING PIECE  
IN NEHASHI SABURO; FUJISAKI MASANOBU; NAKAMURA HIDEAKI  
PA SEIKO EPSON CORP  
PI JP 2001274128 A 20011005 Heisei  
AI JP 2000-168817 (JP2000168817 Heisei) 20000606  
PRAI JP 2000-13579 20000121  
SO PATENT ABSTRACTS OF JAPAN (CD-ROM), Unexamined Applications, Vol. 2001  
IC ICM H01L021-304  
ICS B24B037-00; H03H003-02  
AB PROBLEM TO BE SOLVED: To polish a piezoelectric material, such as quartz or other brittle thin sheet into a very thin sheet, without damaging it, and to polish a piezoelectric wafer to a thickness of about 10-25  $\mu$ m or less to realize a high frequency piezoelectric vibrator of about 70-160 MHz or higher.  
SOLUTION: Two quartz crystal wafers are bonded mutually directly or through a dummy sheet with photosetting adhesives into a laminate wafer, and both sides of the laminate wafer are polished to a desired thickness, using the conventional carrier and polisher. Prior to or after processing the polished laminate wafer into vibrating pieces of a desired overall size, it is immersed in a releasing liquid to dissolve the adhesives, thereby separating into individual vibrating pieces. If many recesses are previously formed beforehand into the bonding faces of the quartz wafers or dummy sheet, corresponding portions of the quartz wafers to the recesses bend during polishing and recover their initial state to project to the opposite side after processing, thus easily obtaining inverted mesa type AT cut piezoelectric vibrating piece which have very thin wall vibrating parts with protruding sections. COPYRIGHT: (C)2001, JPO

L46 ANSWER 4 OF 12 WPIX COPYRIGHT 2005 THE THOMSON CORP on STN

AN 1996-210818 [22] WPIX Full-text

DNN N1996-176409

TI Manufacturing ink jet head for computer printer - having supporting member with recesses corresponding to substrates into which adhesive material is supplied.

DC P75 S06 T04 W02

IN HARUYAMA, H; IKETANI, M; KARITA, S; KASHINO, T; KOIZUMI, Y; OMATA, K; SAWADA, Y; TAJIMA, H; TERAI, H

PA (CANO) CANON KK

CYC 13

PI EP 709202 A2 19960501 (199622)\* EN 30 B41J002-16

R: AT DE ES FR GB IT NL

AU 9534572 A 19960523 (199628) B41J002-155

EP 709202 A3 19970416 (199729) B41J002-16

SG 40043 A1 19970614 (199732) B41J002-16

JP 09183229 A 19970715 (199738) 16 B41J002-16

CN 1134361 A 19961030 (199803) B41J002-135

AU 691036 B 19980507 (199830) B41J002-155

US 5826333 A 19981027 (199850) B41J002-16

KR 156449 B1 19981201 (200032) B41J002-135

EP 709202 B1 20020703 (200243) EN B41J002-16

DE 69527246 E 20020808 (200259) B41J002-16

US 6499828 B1 20021231 (200305) B41J002-155

JP 3517498 B2 20040412 (200425) 15 B41J002-16

CN 1058660 C 20001122 (200472) B41J002-135

PRAI JP 1995-281618 19951031; JP 1994-267057

19941031

AB EP 709202 A UPAB: 19970922

The method of manufacturing an ink jet head involves arranging several substrates which have ejection energy generating elements on a supporting member. A top plate is mounted on the supporting member so as to cover all the substrates and form ink flow paths. The supporting member includes recesses at a supporting portion.

An adhesive material is supplied to the recesses and after this the substrate is placed on the supporting member. The supporting member includes openings corresponding to the substrates. The substrates are sucked through the openings so as to be temporarily fixed.

USE/ADVANTAGE - For colour printing. For copier or facsimile. For textile printing. Stable due to avoiding cross talk. Uniform printing quality. High resolution. Reliable. Dwg.1/24

FS EPI GMPI

FA AB; GI

MC EPI: S06-A11; S06-A16B; T04-G02; T04-G07; W02-J02B3; W02-J04